AN-SM2203

600V *e*MOS E7 Series

Well Balanced Power Master Semiconductor's Super-Junction MOSFET Technology

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1. Introduction

This document describes Power Master Semiconductors' 600V super-junction MOSFET, eMOS E7 series. This new super-junction, eMOS E7 opens the door to power converter designers for targeting high efficiency and ease of use. The eMOS E7 enables to offer cost-effective, high performance and robust solution for AC/DC and DC/DC applications such as PFC, and hard & soft switching topologies. This application note describes the key parameters and benefits of 600V eMOS E7 series compared to competitor devices.

1.1. What is super-junction MOSFET?

The major contribution to $R_{DS(ON)}$ of high-voltage MOSFET (>500V) comes from the epi layer. The portion of epi resistance is higher for high breakdown voltage MOSFETs due to the higher resistivity or lower carrier concentration in the epi layer. Therefore, epi resistance should be decreased for the lower $R_{DS(ON)}$·Q_G, Figure of Merit(FOM) for high voltage MOSFETs. The super-junction technology utilizing charge balance technology is widely used for high voltage Si MOSFETs to overcome the limit of silicon. Figure 1 shows vertical structure and electric field profile of a conventional planar MOSFET and super-junction MOSFET. Breakdown voltage of the planar MOSFET is determined by drift doping and its thickness. The slope of electric field distribution is proportional to drift doping. Therefore, thick and lightly doped epi is needed to support higher breakdown voltage. Super-junction technology has long p-type pillar structure in the body. The effect of the p-type pillars is to enable the electric field to become flat in the lightly doped epi region.
Therefore, super-junction technology can increase breakdown voltage with same doping and epi thickness by larger electric field area thanks to p-type pillar in figure 1. In other words, a much lower specific on-resistance can be achieved with super-junction structures by increasing the N-drift dose while maintaining same breakdown voltage.

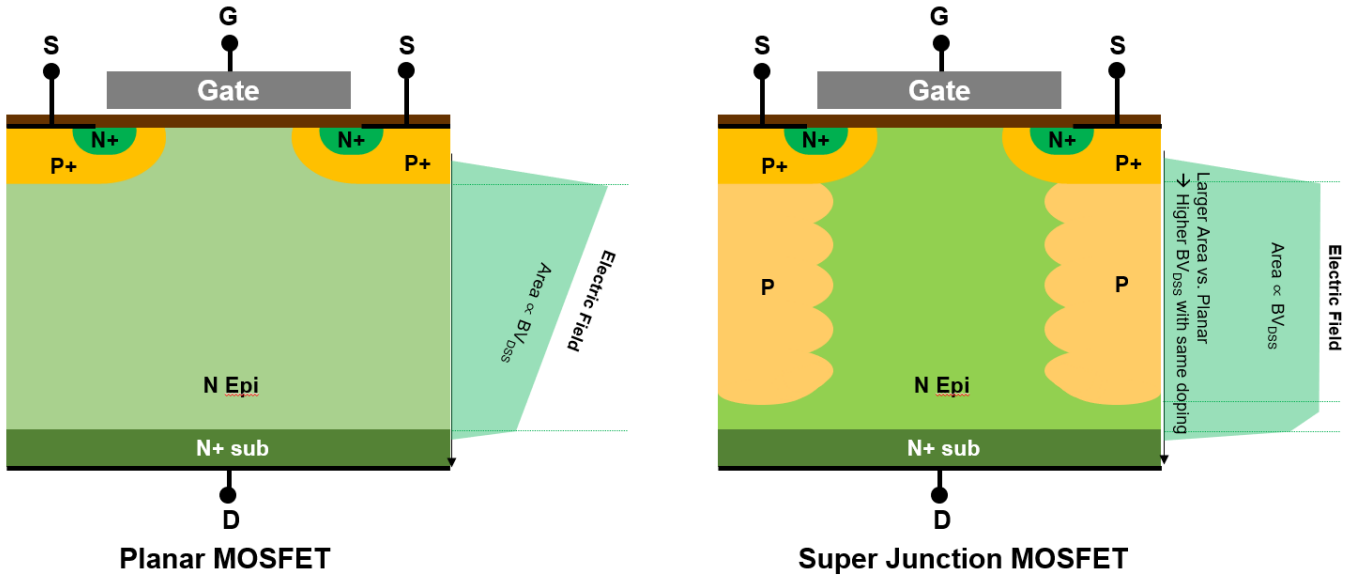


Figure 1. Vertical structure and electric field profile : planar MOSFET vs super-junction MOSFET

2. 600V eMOS Technology

High voltage super-junction MOSFET (> 500V) is widely using in many power conversion systems such as AC/DC, DC/DC, DC/AC applications. Power Master Semiconductor introduced the 600V eMOS E7 as leading-edge super-junction technology for targeting high efficiency, reliable and ease of use in hard and soft switching topologies.

2.1. Target Applications

As shown in figure 2, The eMOS E7 series is designed to target the world-class performance in the various applications such as adaptors, PC powers, TV powers (LCD / LED / OLED), server / telecom powers, PV inverters, EV chargers for DC EV charging piles and on-board chargers.

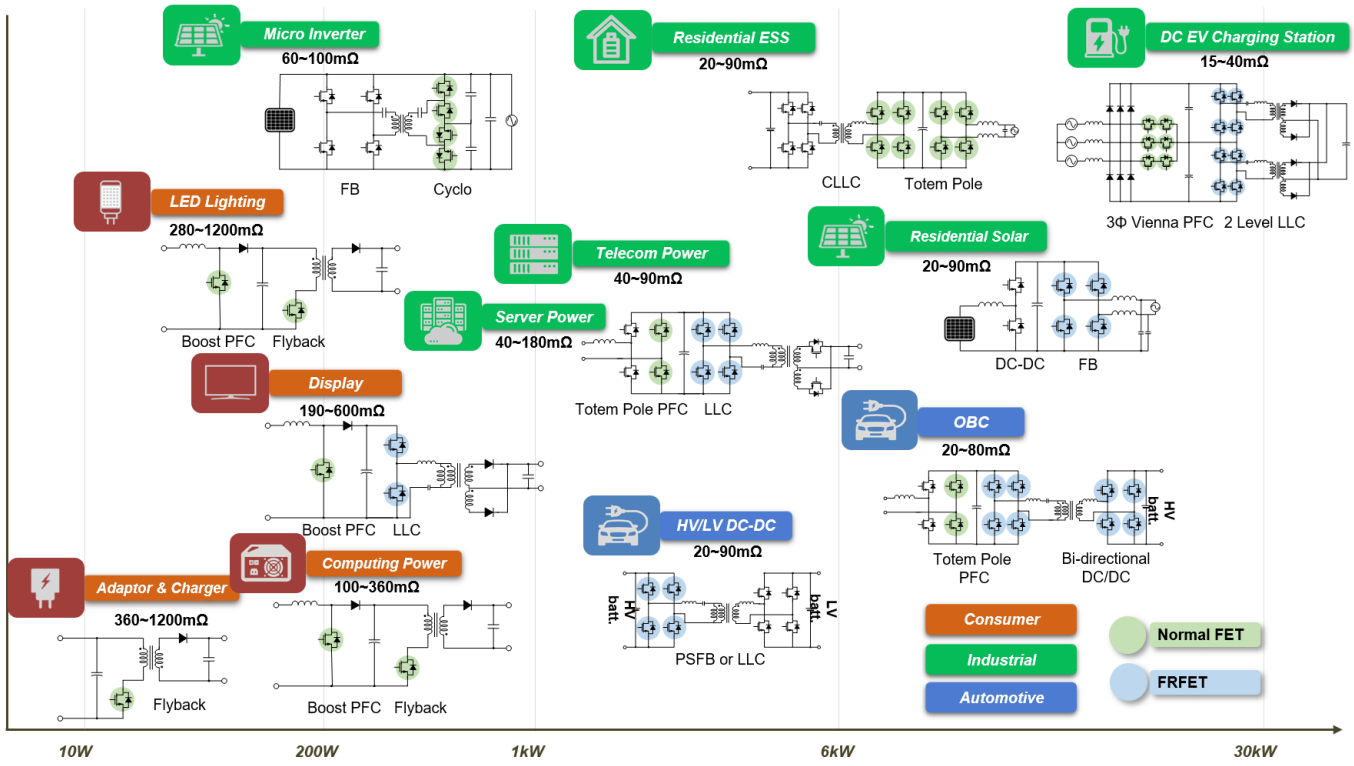


Figure 2. 600V eMOS 7 Series - Target applications

2.2. 600V eMOS E7 – Features and Benefits

The target performance of 600V eMOS E7 series is to provide a well-balanced trade-off between switching losses and switching spikes / oscillation by optimized parasitic capacitances without internal R_G. Therefore, 600V eMOS E7 provide more freedom to designer in selecting external R_G for power conversion systems. It enables to offer high performance, cost-effective, and robust solution with a wide range of package options. As shown in figure 3, The 600V eMOS E7 series has highly optimized key performance for both hard-switched boost PFC switch and primary switch of a soft switched LLC resonant topologies.

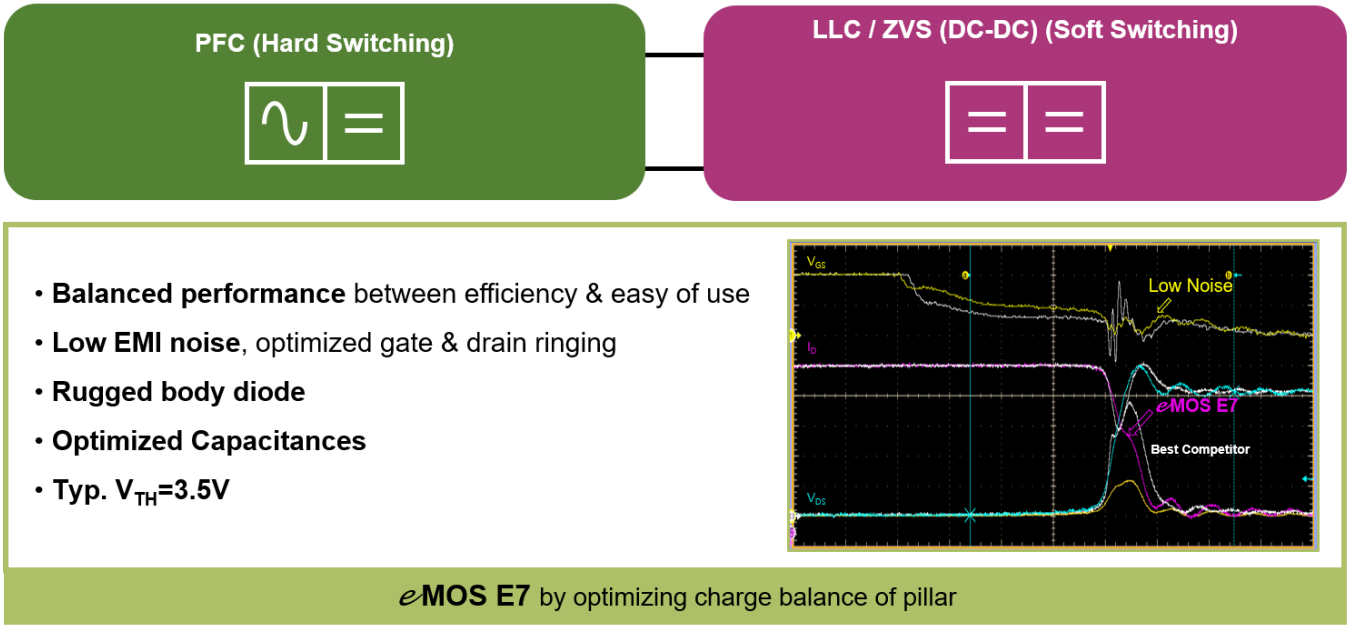


Figure 3. *e*MOS's optimized performance for both hard and soft switching topologies

The 600V *e*MOS E7 is an advanced Power Master Semiconductor's super-junction MOSFET family by utilizing charge balance technology for excellent low on-resistance and gate charge. This technology combines the benefits of fast switching performance with lower switching noise and spikes and robustness.
Robust intrinsic body diode performance of 600V *e*MOS E7 provide better reliability in soft switching topologies such as LLC resonant converters or ZVS phase-shifted full bridge converters.
Consequently, the *e*MOS E7 family is suitable for many applications requiring superior efficiency and higher power density.

Key Features

- Excellent ruggedness
- Good switching behavior for hard and soft switching.
- Significant reduction of switching and conduction losses

Key Benefits

- Suitable for hard and soft switching (PFC and LLC)
- Ease of use and fast design-in through low ringing tendency and usage across PFC and PWM stages
- Simplified thermal management due to low switching and conduction losses
- Suitable for a wide variety of applications and power ranges

2.3. 600V *e*MOS E7 – Key Electrical Characteristics

The key electrical parameters of 600V *e*MOS is compared to those of three competitor devices (including the best competitor). Power Master Semiconductor's the first-generation super-junction MOSFET, 600V *e*MOS E7 has very competitive performance against the latest generation of competitor's super-junction MOSFETs.

Table 1 shows the key parameter comparison of Power Master Semiconductor's 600V/180mΩ eMOS E7 and the competitor's the latest super-junction MOSFETs. 600V eMOS E7 shows the best avalanche capability (I_{AS}) with very competitive FOM against the latest competitors and guarantee very high MOSFET dv/dt(100V/ns) and peak diode recovery dv/dt(20V/ns) for better system design margin.

Table 1. Key parameter comparison of Power Master Semiconductor's 600V/180mΩ eMOS and the competitor.

Specification	PMF60N180E7	Comp. A	Comp. B	Comp. C
BV_{DSS}	600 V	600 V	600 V	650 V
I_D	19 A	18 A	20 A	17 A
I_{DM}	57.0 A	53.0 A	60.0 A	42.5 A
$R_{DS(on)}$ Max	180 mΩ	180 mΩ	190 mΩ	190 mΩ
Q_G	30.2 nC	25.0 nC	36.0 nC	33.0 nC
FOM [$R_{DS(on)}$·Q_G]	5.4 Ω·nC	4.5 Ω·nC	6.8 Ω·nC	6.3 Ω·nC
V_{TH} (Min. / Max.)	2.5V / 4.5V	3.0V / 4.0V	2.0V / 4.0V	2.5V / 4.5V
Q_{RR}	3.3 µC	1.3 µC	5.3 µC	4.9 µC
Internal R_G	1.3 Ω	11.0 Ω	8.0 Ω	0.5 Ω
MOSFET dv/dt	100 V/ns	80 V/ns	50 V/ns	100 V/ns
Peak Diode Recovery dv/dt	20 V/ns	50 V/ns	15 V/ns	20 V/ns
I_{AS} @ L=12µH	19.6 A	13.6 A	13.8 A	18.1 A

2.4. 600V eMOS E7 – Competitor Benchmark

Figure 4 shows the 600V eMOS E7 performance position against the latest competitors. As shown in this spider chart, 600V eMOS E7 offers very low switching losses with the best-in-class avalanche ruggedness against the latest generation of competitor's super-junction MOSFETs. 600V eMOS E7 has high I_{DM} capability. Higher I_{DM} (pulse current) capability is required for more design margin from customer side for abnormal operation test such as start-up, AC drop out test, output short and so on. The low Q_G of 600V eMOS can reduce driving loss that is critical in light load efficiency. Thanks to excellent body diode performance (low Q_{RR} and robust body diode ruggedness) of 600V eMOS E7 technology it is suitable for not only hard switching topologies but also soft switching topologies such as ZVS phase-shifted full bridge or LLC resonant converters. 600V eMOS' E7's outstanding parameters result in the higher system efficiency and reliability in target applications.

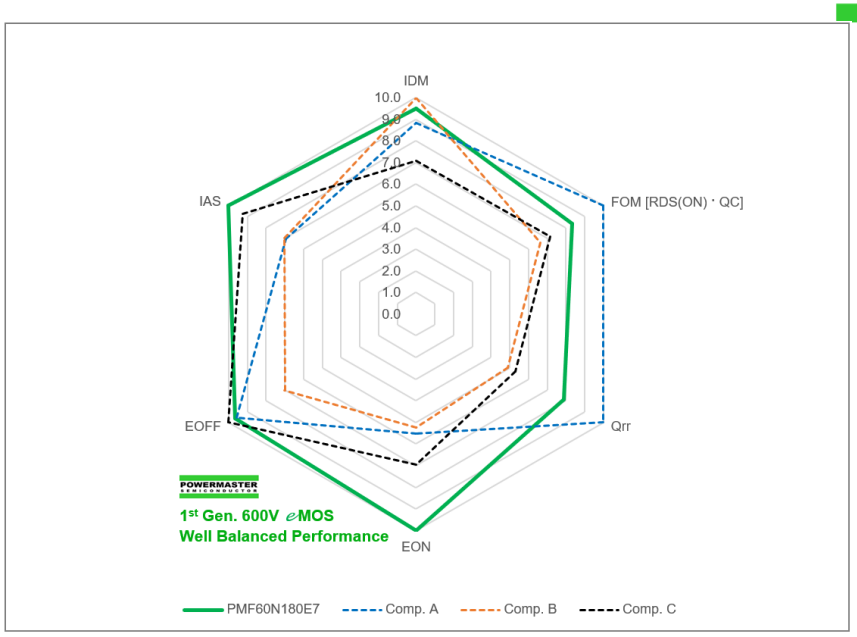
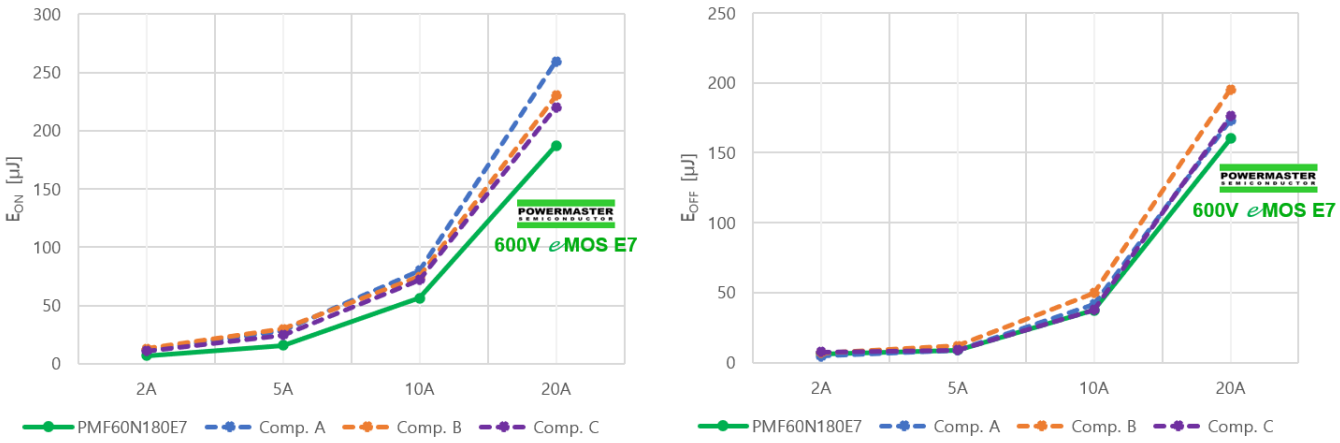


Figure 4. 600V/180mΩ *e*MOS E7 performance position against the latest competitors (Note1: 10 is the best, 0 is the worst)

2.5. 600V *e*MOS E7 – Switching Characteristics

Figure 5 shows switching losses (E_{ON} and E_{OFF}) comparison for 600V/180mΩ *e*MOS E7 vs competitors under same test conditions, V_{DD}=400V, I_D=2~20A, V_{GS}=10V, R_G=8.2Ω. Switching losses of 600V *e*MOS E7 are reduced compared to that of competitor's devices. Figure 6 shows the turn-off dv/dt comparison between 600V/180mΩ *e*MOS E7 and competitors. 600V *e*MOS E7 and competitor A are very well controlling dv/dt that is limited to ~55V/ns at high current operation. But the dv/dt of competitor B and C is linearly increased up to 95~100 V/ns at high current (I_D=20A). To summarize, 600V *e*MOS E7 has well balanced switching trade-off (switching losses vs switching dv/dt) at low and high current operation.



(a) Turn-on switching loss (E_{ON}) comparison (b) Turn-off switching loss (E_{OFF}) comparison

Figure 5. 600V/180mΩ *e*MOS E7 switching loss comparison under V_{DD}=400V, I_D=2~20A, V_{GS}=10V, R_G=8.2Ω. at inductive load switching.

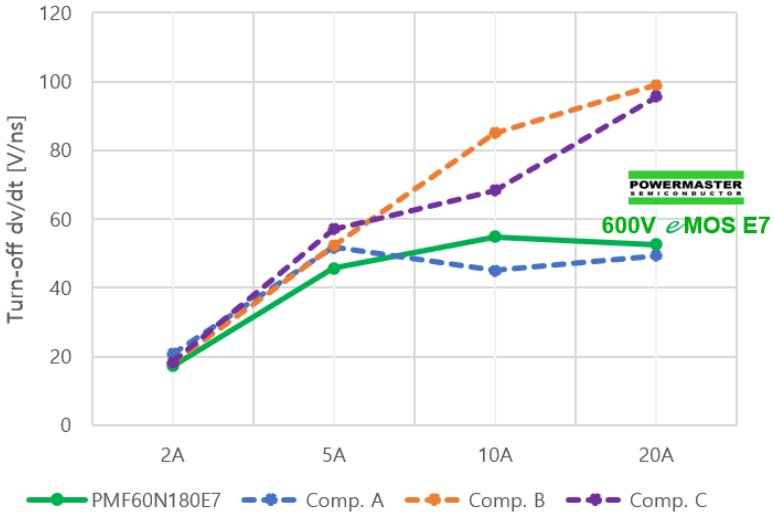


Figure 6. 600V/180mΩ eMOS E7 turn-off switching dv/dt comparison under V_{DD}=400V, I_D=2~20A, V_{GS}=10V, R_G=8.2Ω. at inductive load switching.

Figure 7 shows switching waveform comparison for 600V / 70mΩ eMOS E7 vs the best competitor under V_{DD}=400V, I_D=15A, V_{GS}=10V, R_G=4.7Ω (color : PMW60N070E7, white : the best competitor). The cross−over area of the drain−source voltage and drain current, Turn-off loss of PMW60N070E7 (67μJ) is 20% less than the best competitor (84μJ) at I_D=15A. Generally, switching dv/dt, di/dt is highly affected by parasitic components of packages and PCB. High dv/dt and di/dt lead to gate oscillation that influence each other. Thanks to optimized pillar design of 600V eMOS E7, the dv/dt of PMW60N070E7 (61V/ns) is 46% lower than that of the best competitor (95V/ns) at I_D=15A while reducing switching losses. Furthermore, the gate oscillation (yellow) of PMW60N070E7 is much reduced compared to the best competitor under same test board and condition. Therefore, 600V eMOS E7 has highly optimized switching performance (switching efficiency and noise).

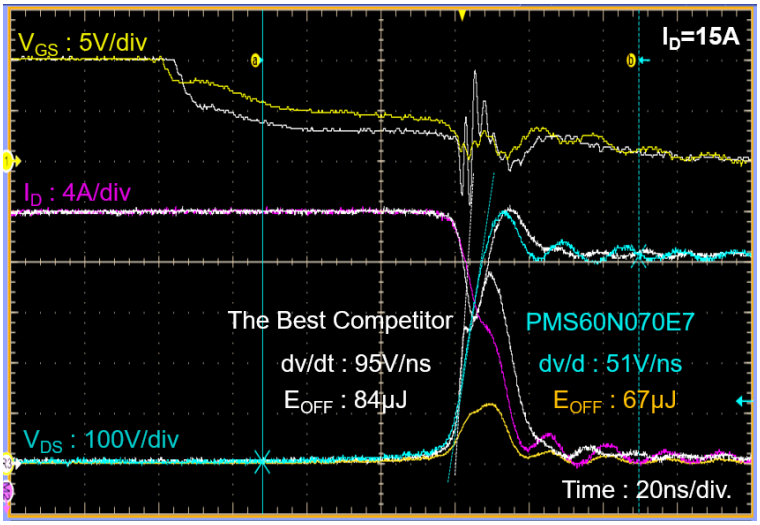


Figure 7. 600V / 70mΩ eMOS E7, turn-off switching waveform comparison under V_{DD}=400V, I_D=15A, V_{GS}=10V, R_G=4.7Ω. at inductive load switching. (Color : PMW60N070E7, White : The best competitor)

2.6. 600V eMOS E7 – Avalanche Capability

Generally, SMPS (Switching Mode Power Supply) should be designed to keep V_{DS} below the BV_{DSS} rating, and 80% derating is used in normal operation of SMPS. But peak V_{DS} can exceed 100% during abnormal operation and device can be failed avalanche breakdown mode. As shown in figure 8, when the Power MOSFET avalanches, the drain-source voltage is clamped to its effective breakdown voltage and the current is commutated through a P-N junction of body diode. In addition to this process, high dv/dt affects to build up more displacement current. The displacement current is added to avalanche current and the device becomes more vulnerable to failure. Basically, the root cause of failure is parasitic BJT trigger due to high current and temperature. Therefore, device avalanche capability is critical under abnormal operation.

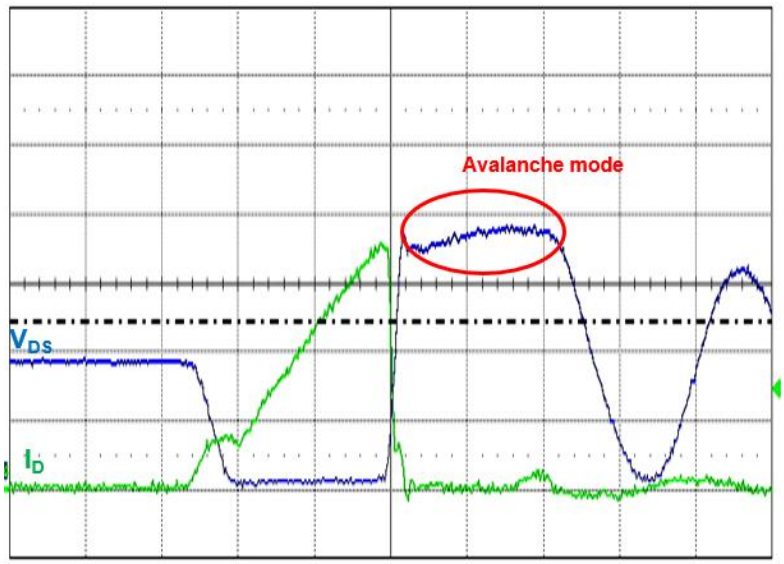
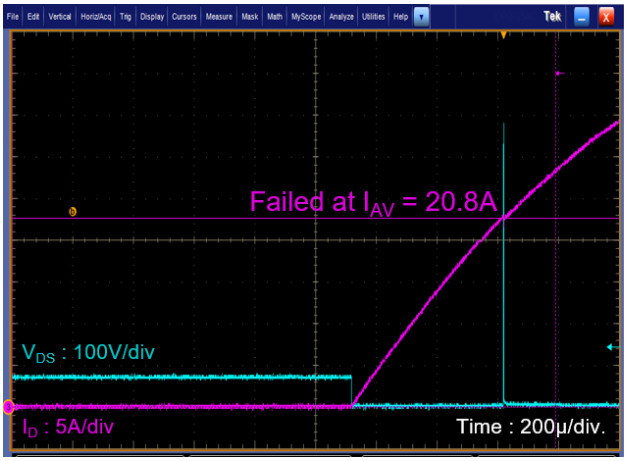
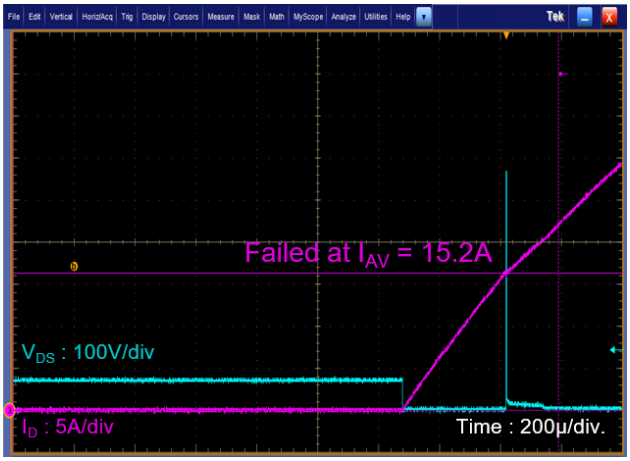


Figure 8. MOSFET avalanche breakdown mode in SMPS

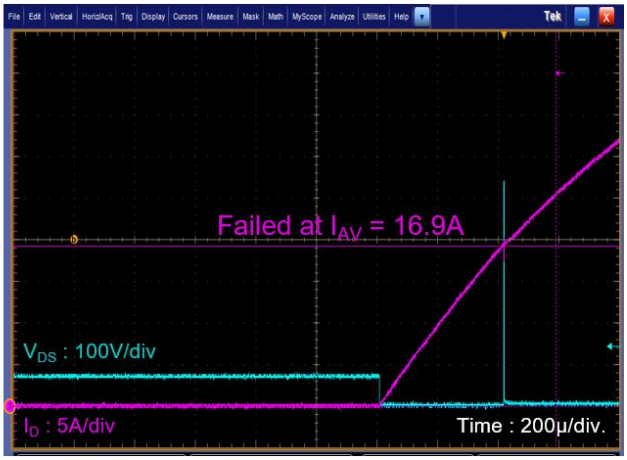


(a) PMW60N099E7 (600V / 99mΩ)



(b) Competitor I (600V / 99mΩ)

(c) Competitor II (650V / 99mΩ)



(d) Competitor III (650V / 95mΩ)

Figure 9. 600V / 99mΩ eMOS E7 avalanche comparison under V_{DD}=70V, V_{GS}=10V, R_G=25Ω and L=1mH.

Figure 9 shows avalanche capability comparison for 600V / 99mΩ eMOS E7 and various competitor's super-junction MOSFETs under V_{DD}=70, V_{GS}=10V, R_G=25Ω and L=1mH. With competitors devices(same or similar $R_{DS(ON)}$), avalanche breakdown failure occurs around 15~17A (average value among 5 samples) and 600V / 99mΩ eMOS E7 failed at 20.8A (average value among 10 samples) under same test condition. 600V / 99mΩ eMOS E7 provides the best-in-class avalanche capability for system reliability under abnormal operations.

2.7. 600V eMOS E7 – System Benchmark

System efficiency of 600V / 180mΩ eMOS E7 is compared to 600V / 180 or 190mΩ competitor devices in CCM PFC of 500W server power supply. Operating frequency is 65kHz. As shown in figure 10, 600V eMOS E7 shows the best efficiency at full load and balanced efficiency at light and medium load conditions. By replacing the 600V eMOS E7, system efficiency increases about 0.13% than competitor C at light load and 0.16% than competitor B at heavy load respectively. In figure 11, an infrared camera was used to measure device temperature. Thanks to the best performance of 600V eMOS E7 at full load condition, temperature of 600V eMOS E7 is lower than the competitor B by around 10 degrees. Finally, 600V eMOS E7 can maximize switching efficiency and minimize switching noise to offer excellent system efficiency and easy to use with high ruggedness for better system reliability.

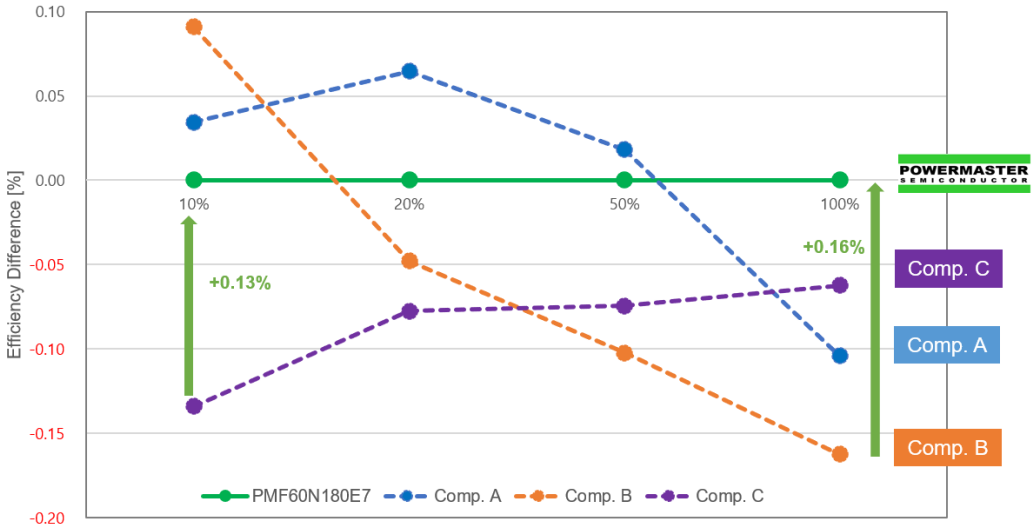


Figure 10. Relative efficiency comparison 600V/180mΩ eMOS E7 and competitors at CCM PFC block of 500W server power supply, V_{IN}=110V, 60Hz

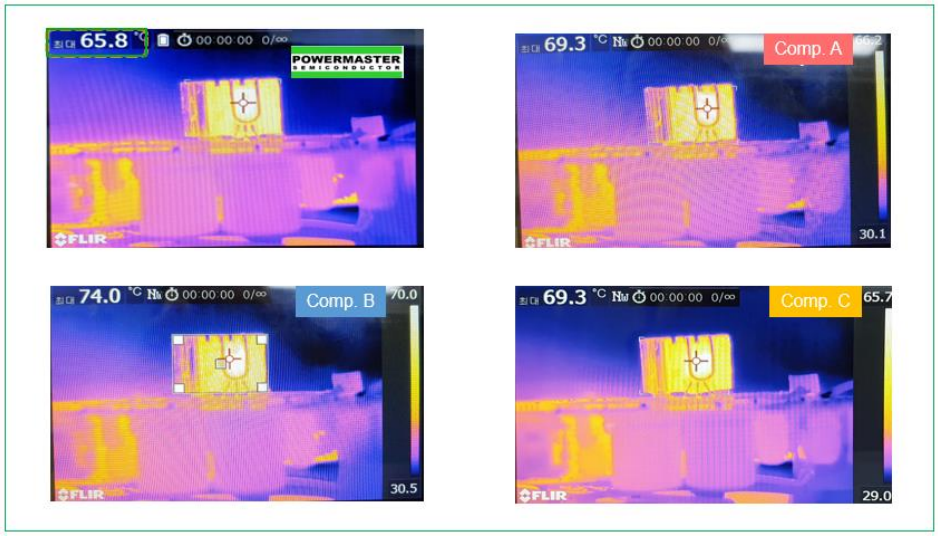


Figure 11. MOSFET case temperature comparison 600V/180mΩ eMOS E7 and competitors at CCM PFC block of 500W server power supply, V_{IN}=110V, 60Hz, full load.

3. Conclusion

Power Master Semiconductor's the first generation of super-junction MOSFET, 600V eMOS E7 series is designed to target the world-class performance in the broad range of applications ranging from low power up to the high power applications. The eMOS is well-balanced in terms of combining ease of use (e.g. low ringing) with an excellent efficiency performance and a reasonable price. The eMOS offers outstanding performance of lower switching losses without sacrificing switching noise, robust body diode and avalanche capability in hard-switching and soft-switching topologies for high efficiency and high power density power conversion system.

4. 600V eMOS Product Portfolio & Nomenclature

4.1. 600V eMOS Product Portfolio

Table 1. 600V eMOS Product Portfolio

eMOS E7 (Efficient)
for PFC & LLC Topologies

Adaptor | ATX Power | Class-D Audio | TV / LED Lighting | Solar | Server / Telecom | UPS | EV Charger | EV(OBC)

PKG / $R_{DS(ON)}$ max	Die	DPAK	PQFN88	TO-220	TO-220F	TO-247 3L
28mΩ						PMW60N028E7(-A)
40mΩ						PMW60N040E7(-A)
70mΩ						PMW60N070E7(-A)
99mΩ			*PML60N105E7(-A)	PMP60N099E7(-A)	PMF60N099E7(-A)	PMW60N099E7(-A)
120mΩ						
180mΩ	PMO60N180E7(-A)			PMP60N180E7(-A)	PMF60N180E7(-A)	
280mΩ	PMO60N280E7(-A)	PMD60N280E7(-A)		PMP60N280E7(-A)	PMF60N280E7(-A)	
380mΩ	PMO60N380E7(-A)	PMD60N380E7(-A)		PMP60N380E7(-A)	PMF60N380E7(-A)	
600mΩ	PMO60N600E7(-A)	PMD60N600E7(-A)			PMF60N600E7(-A)	

* Coming soon
(-A : Automotive Grade)

For more product information, please visit https://www.powermastersemi.com

4.2. Nomenclature

Device part number contains a lot of information such as technology, package, voltage rating and generation, etc. Figure 12 shows Power Master Semiconductor's super-junction MOSFET, eMOS nomenclature

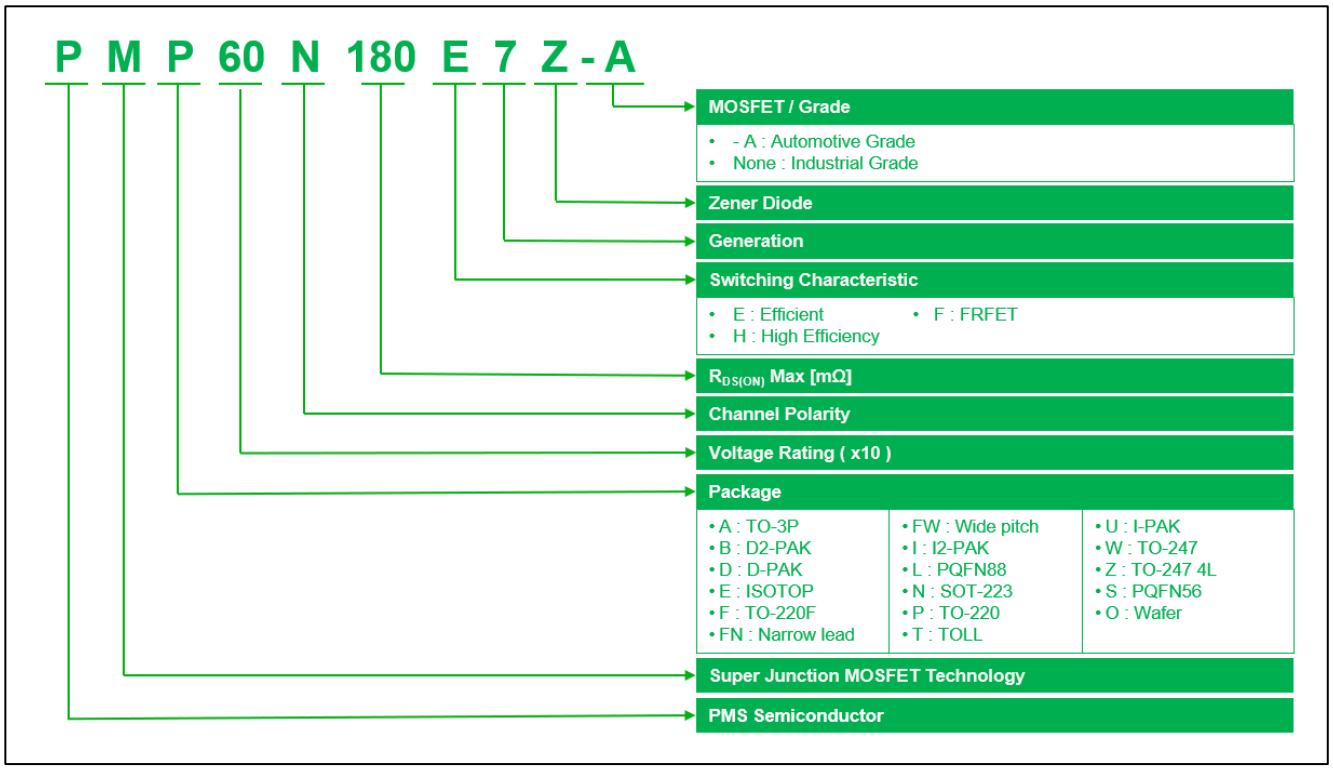


Figure 12. eMOS nomenclature scheme

5. Document Revision History

Major changes since the last version

Date	Description of change
09-Aug-2022	First Release

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